Integrated Transceiver Arrays for Multiple Antenna Systems

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***Abstract*—In this paper, we present area-efficient multiple antenna transceiver front ends. A portion of the greatly increased capacity (compared to a single antenna system) of the multiple antenna system is traded off for relaxed circuit noise requirements. This allows circuits without physically large on-chip inductors to be used, resulting in significant chip area savings. Comparing the area and noise performance between a narrowband low noise amplifier (LNA) and a broadband LNA shows a simulated 3 dB increase in noise figure but a threefold decrease in area. Furthermore, multiple receiver front ends for a proposed four transmit, four receive antenna (4x4) system have a smaller area than some reported single front ends.**

Keywords -multiple antennas; broadband circuits; transceiver

I. INTRODUCTION

With the dawn of 802.11n, arrays of multiple antennas at the transmitter and receiver promise a greatly increased capacity without increasing the required bandwidth. Going from a single transmit, single receive antenna (1x1) system to a four transmit, four receive antenna (4x4) system potentially allows a quadrupling of the capacity. However, each antenna requires an analog transceiver front end. Putting each front end on a separate chip is costly as the number of antennas continues to increase. Integration of the parallel RF chains onto a single chip is a cost effective solution when the large Signal-to-Noise Ratio (SNR) gains available with multiple antennas allow much smaller circuits to be used. The reduction in required SNR makes possible wireless systems that otherwise could not be built (e.g., due to excessive transmit power).

A current research effort at the Massachusetts Institute of Technology is the development of a Wireless Gigabit Local Area Network (WiGLAN). The WiGLAN operates at 5.25 GHz and achieves gigabit per second data rates through the use of 150 MHz bandwidth, Orthogonal Frequency Division Multiplexing (OFDM), and adaptive modulation. Depending on the SNR for each OFDM bin, the modulation per bin varies from 4-QAM to 256-QAM. As a multiple antenna system, the WiGLAN uses parallel radios with space-time coding and processing to exploit the spatially independent fading that exists in a rich scattering environment. Although able to further increase the data rates through spatial multiplexing, the WiGLAN's primary use of multiple antennas is to provide spatial diversity that allows for an expanded range, lower transmit RF power, and, as covered in this paper, area-efficient circuit implementations of multiple antenna systems. With the WiGLAN, appliances throughout the home or office environment can communicate wirelessly among themselves and to a central network controller. Depending on the needs and type of each node, single and multiple antenna portable adapters are attached to the various appliances. Devices that require high data rates and excellent link quality for large ranges (e.g. an HDTV or DVD player) use multiple antennas while short range, low data rate appliances use single antennas.

At first glance, an individual front end per antenna seems to suggest that the area and DC power consumption increase proportionally with the number of antennas. Thus, for example, a receiver with four antennas consumes four times the area and DC power of a one-antenna receiver. Area is a major consideration for on-chip designs because it translates directly to chip fabrication cost and, for larger die area, results in fewer chips per wafer. Likewise, for portable applications, higher DC power consumption results in shorter battery life. However, large SNR gains, which are available through spatial diversity with multiple antenna systems, can potentially allow area- and power-efficient circuits to be used. Several possible tradeoffs are as follows. One tradeoff uses the SNR gain to relax the noise requirement of the receiver. This allows noisier but physically smaller inductor-less circuits to be used. Another applies the SNR gain to lower the necessary transmit power. A third potential tradeoff, currently under investigation, minimizes DC power consumption by operating circuits at a lower current but accepting a degraded noise performance.

The rest of this paper is organized as follows. Section II briefly introduces parallel radio systems and presents the SNR gain achievable with multiple antennas. It then shows through a link budget analysis how SNR gain can allow for a relaxed circuit noise performance. Section III presents two low noise amplifier (LNA) designs and discusses the issue of using on-chip passive components. Section IV compares the areas and noise figures for several single receiver front ends in the literature with a proposed multiple receiver front end and shows that the latter design is comparable for both aspects. Section V concludes the discussion.

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II. THE SYSTEM MODEL AND PERFORMANCE MEASURES

A. Wireless Capacity and Bit Error Rate

In a rich scattering environment of an indoor wireless channel, there exist parallel sub-channels in space that create multiple channel inputs and outputs. Due to multi-path, each transmit antenna can simultaneously transmit with the same frequency band because it effectively sees a different channel. Channel matrix knowledge allows the receiver to extract the spatial signatures of the transmitted signals. For a system with M transmit and N receive antennas, the capacity C is [1]

$$C = E\left[\sum_{i=1}^{M}\log_2(1+\lambda_i SNR)\right] \approx k\log_2(\beta SNR), \qquad (1)$$

where λ_i are the eigenvalues of $\mathbf{H}^T\mathbf{H}$, SNR is the received signal-to-noise ratio, $\mathbf{H}$ is a NxM channel matrix, and the expectation is over all $\mathbf{H}$. The approximation is valid in the high SNR regime, with k=min(M,N) being the number of degrees of freedom for the system (assuming $\mathbf{H}$ is full rank), and β a constant that depends on the specific structure of $\mathbf{H}$. For any two capacities C_1 and C_2 in the high SNR regime, the change in capacity ΔC with respect to SNR is

$$\Delta C = C_2 - C_1 \approx k\log_2\left(\frac{\beta SNR_2}{\beta SNR_1}\right) = k\Delta SNR. \qquad (2)$$

Using (2), k b/s/Hz capacity is traded for every 3dB relaxation in SNR. This capacity-diversity tradeoff [2] yields an SNR gain of about 40 dB for the 4x4 system over the 1x1 system. The 4x4 system is able to reduce the required transmit power or relax the necessary receive SNR by a factor of ten thousand compared to a 1x1 system. Since the capacity gains from (2) require complex and computationally expensive coding and more complicated transceiver circuits, we focus instead on the uncoded case and apply maximum diversity gain. Fig. 1 shows a simulation result for the bit error rate (BER) versus SNR for two systems using uncoded 64-QAM in a Rayleigh fading channel. For the 4x4 system, repetition coding across parallel subchannels was used to focus strictly on maximum diversity. The SNR is plotted as E_s/N_o, where E_s and N_o are the average energy and noise power per receive antenna, respectively. For a BER of 10^{-5}, or 1% packet error for 1000 bit long packets, the SNR difference between systems is 40 dB.

B. Link Budget

For wireless circuit designers, a lower SNR requirement translates to a smaller power amplifier (PA) output power, and/or an LNA with a more relaxed input noise requirement. Lowering the output power of the PA not only reduces power consumption, but also increases linearity as the amplifier operates farther from saturation. Furthermore, as shown in Section III, designers could choose to implement broadband circuits that eliminate inductors and thus significantly save chip area. To appreciate these details, an examination of the link budget is necessary.

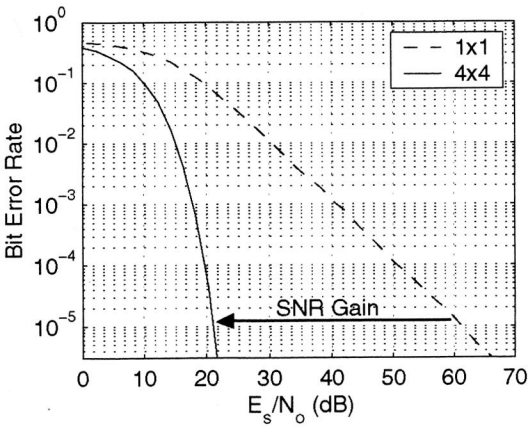

Figure 1. Plot of 1x1 vs. 4x4 BER for a 64-QAM input constellation

At the input of the receiver front end, the average signal power is

$$P_R = P_T - P_L, \qquad (3)$$

where P_R is received power, P_T is transmitted power, and P_L is the path loss (all in dB). The path loss is a function of the carrier wavelength λ, distance d, and path loss exponent n and is given by

$$P_L = 20\log_{10}\left(\frac{\lambda}{4\pi}\right) + 10n\log_{10}\left(\frac{d}{d_o}\right). \qquad (4)$$

Typically, the loss at d_o=1 m is measured and losses at a distance greater than 1 m are related through the second term of (4). The input signal to noise ratio (SNR_i) is given by

$$SNR_i = P_R - (N_i W), \qquad (5)$$

where N_i is the input noise power density in dBm/Hz and W is the noise equivalent bandwidth in Hertz. The electronics add noise to the signal as it is processed, which degrades the SNR. The resulting output SNR_o in dB is then given as

$$SNR_o = SNR_i - NF, \qquad (6)$$

where NF is the noise figure of the electronics. The noise figure captures the circuit noise contribution into a single number that represents the effective loss in SNR. The output SNR_o can be related to E_s/N_o of Fig. 1 through

$$SNR_o = E_s / N_o + 10\log_{10}(R_s / W). \qquad (7)$$

By letting symbol rate equal the bandwidth, that is, $R_s=W$, the noise figure is given as

$$NF = SNR_i - E_s / N_o. \quad (8)$$

Table I shows a sample link budget for a 1x1 system and a 4x4 system using (3)-(5), (8) and Fig. 1. The required noise figures are calculated assuming that a 64-QAM constellation should be decodable at a distance of 10 meters with an uncoded BER of 10^{-5}. This distance is appropriate for a home or office environment, which is the target of the WiGLAN. The transmit power P_T is fixed at 100 mW, or 20 dBm, and the path loss exponent is n=3, which is a reasonable choice for an environment such as an office space with no direct line of sight between the transmitter and receiver. The final result is that the required noise figure at 10 m is 14 dB for a 4x4 system, and –26 dB for a 1x1 system. The negative NF of the 1x1 system implies $SNR_o > SNR_i$, which is not achievable in a realizable system.

III. CIRCUIT IMPLICATIONS

Noise performance is a major constraint on LNA design as it dominates the receiver noise figure. A well-designed bipolar narrowband LNA will have a noise figure less than 2 dB but uses on-chip inductors. Figs. 2 and 3 show the schematics of a narrowband and broadband LNA, respectively. A differential design approach maintains the isolation between front ends necessary for maximal ratio combining. For the narrowband LNA, inductors L1-L6 are used for input and output matching and filtering. For the broadband LNA, all inductors are eliminated. It instead uses resistors RF1 and RF2 to provide input matching and replaces the output matching network with a buffer (Q5, Q6, R6, and R7).

Fig. 4 shows a comparison of the chip area required for on-chip components sized to the values typical for a 5 GHz LNA fabricated in a standard 0.18 µm SiGe BiCMOS. It is clear that the inductors dominate the LNA's size. Transistors and resistors, on the other hand, are relatively small and use comparatively little area. Therefore, a design that reduces the use of inductors (and to a lesser extent capacitors) provides for an area-efficient implementation of multiple front ends on a single chip.

TABLE I. LINK BUDGET FOR 1X1 NARROWBAND AND 4X4 BROADBAND SYSTEM FOR UNCODED 64-QAM AT 10^{-5} BER

Determine Receive Power	
TX power P_T(dBm)	20
Path loss (dB), d=10 m	76.84
RX power/ant P_R (dBm) avg	-56.84
Determine Maximum RX NF	
N_i*W (dBm)	-92.24
SNR_i (dB)	35.39
E_s/N_o 1x1 (dB)	61.3
E_s/N_o 4x4 (dB)	21.3
RX NF (dB) 1x1	-25.91
RX NF (dB) 4x4	14.09

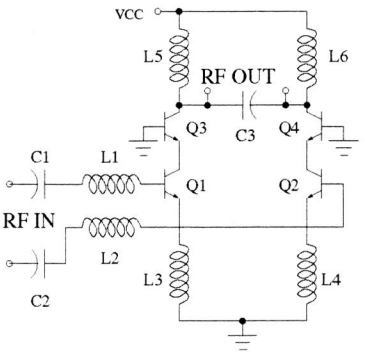

Figure 2. Narrowband LNA

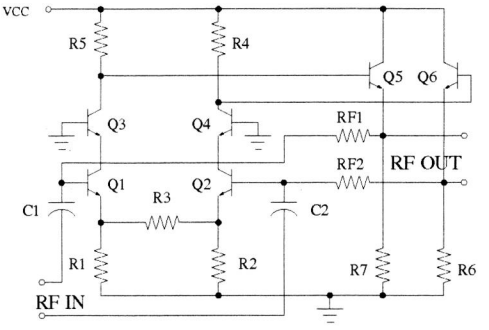

Figure 3. Broadband LNA

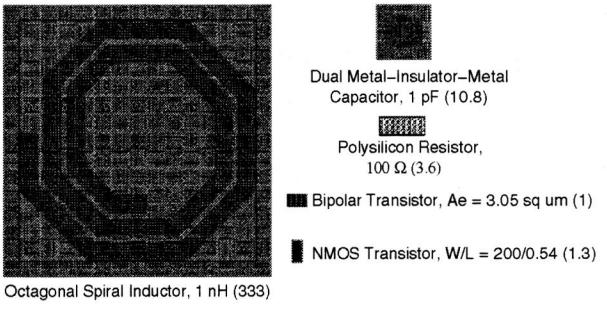

Figure 4. Component sizes (in parentheses) relative to the bipolar transistor

IV. AREA AND NOISE COMPARISONS

To quantify this comparison, both broadband and narrow-band LNAs were designed. The results showed a simulated 1.4 dB noise figure and 0.6 mm^2 area estimate for the narrowband LNA and a simulated 4.4 dB noise figure and 0.23 mm^2 area estimate for the broadband LNA. Thus the broadband approach has a noise figure 3 dB higher than the narrowband approach but occupies roughly one-third the area. Four receiver front ends that incorporated the broadband LNA approach had a simulated noise figure of 8.8 dB and could be implemented on a single chip with a total estimated area of 4 mm^2. This approach has a 3 dB higher noise figure but is only 1.5 times larger than a similar single receiver front end using narrowband circuits. Referring back to Table I, the front

ends have about 5 dB margin from the maximum allowable noise figure for the 4x4 system at 10 meters with uncoded 64-QAM. This margin allows the transmit power to be lowered to 15 dBm, or 32 mW.

Fig. 5 shows that each front end consists of fully differential circuits that include the LNA, image reject filter, mixer, and local oscillator buffer. Although an individual front end is required per antenna, the support circuits are shared. Bias, control, and local oscillator circuits are not duplicated, thus saving DC power consumption and area.

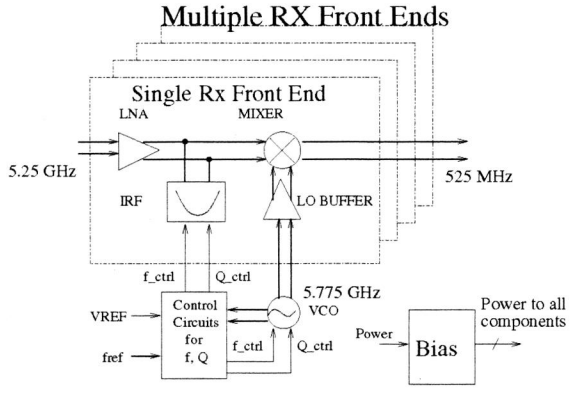

Figure 5. WiGLAN integrated parallel receiver front ends

Table II compares the estimated area and simulated noise figure of the multiple receiver front ends with several 5 GHz single receiver front ends. Fitting within 1 mm^2 and exhibiting a noise figure of 5.2 dB, [3] provides both the lowest noise figure and smallest area of the single front ends considered. The die micrograph visibly shows a tightly packed LNA, filter, mixer plus buffers, image reject phase-locked loop (PLL) and voltage-controlled oscillator (VCO). With more than half of the active chip area occupied by inductors, this chip has tremendous potential to be even smaller. Using a double quadrature receiver, [4] contains an LNA, quadrature generator, mixer, VCO, and polyphase filter on a 3 mm^2 die area. Numerous inductors are visible on the die micrograph but more noticeable are significant "open" spaces surrounding the inductors that appear to consume a third of the active area. It is generally accepted that a certain amount of empty space is left between an inductor and its nearest component to minimize coupling. The actual space depends on the technology and the designers' tolerance level for coupling. The high noise figure for [4] most likely is due to the LNA, which has a noise figure of 4.36 dB. For [5], [6] and [7], a complete transceiver front end exists on chip. However, to be fair, the area of each is an approximation that considers only the receive side. In [5], a 6 mm^2 receiver front end consists of an LNA, image reject filter, mixer, and buffer. A VCO straddles both the transmitter and receiver. The area consumption of this chip does not appear to be optimized, as there appears to be unused spaces surrounding the design. Reference [6] implements a direct conversion receiver and attempts to solve some problems inherent to direct conversion approaches through use of digital calibration. The calibration, which includes programmable gain amplifiers, tunable baseband filters, and an on-chip LO generator, accounts for the majority of the 12.5 mm^2 chip real estate. With a double conversion receiver, [7] sets the second intermediate frequency (IF) at baseband, that is, a direct conversion after the first IF. The receiver front end consists of an LNA, three mixers, and several variable gain amplifiers. Considering the receiver section and the synthesizer, the active area for the receive side is approximately 14 mm^2. Noise figures for [6] and [7] are 5.2 dB and 8.0 dB, respectively. As expected, this paper's proposed multiple front ends based upon broadband circuits exhibit higher noise figure than the approaches in [3]-[7] which use narrowband circuits but occupy an area considerably less than some single front ends.

TABLE II. AREA AND NOISE COMPARISONS FOR 5 GHZ RECEIVER FRONT ENDS

Reference	*Area (mm^2)*	*NF (dB)*
[3]	1	5.2
[4]	3	8.5
This work	4	8.8[b]
[5]	6[a]	5.9
[6]	12.5[a]	5.2
[7]	14[a]	8.0

a. Approximate receiver area for combined transceiver chip; b. Simulation result.

V. CONCLUSIONS

Multiple antenna systems have a potential for large data capacity but the parallel circuitry required can be prohibitively expensive. Trading off some of the increased capacity of the multiple antenna system reduces the SNR required. This leads to lower transmit power and/or area savings through an inductor-less design approach. Circuit and layout techniques can reduce the area further, allowing the proposed multiple front ends to be even smaller. Thus a multiple antenna system is far less costly to implement than expected.

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